

# Exhibit P

### **MacInnis 8,284,844 Applied to Representative Panasonic and Toyota Accused Products**

This claim chart compares independent claim 1 of U.S. Patent No. 8,284,844 (“the MacInnis ’844 patent”) to Texas Instruments’ (“TI”) DRA750 system on a chip (“SoC”).

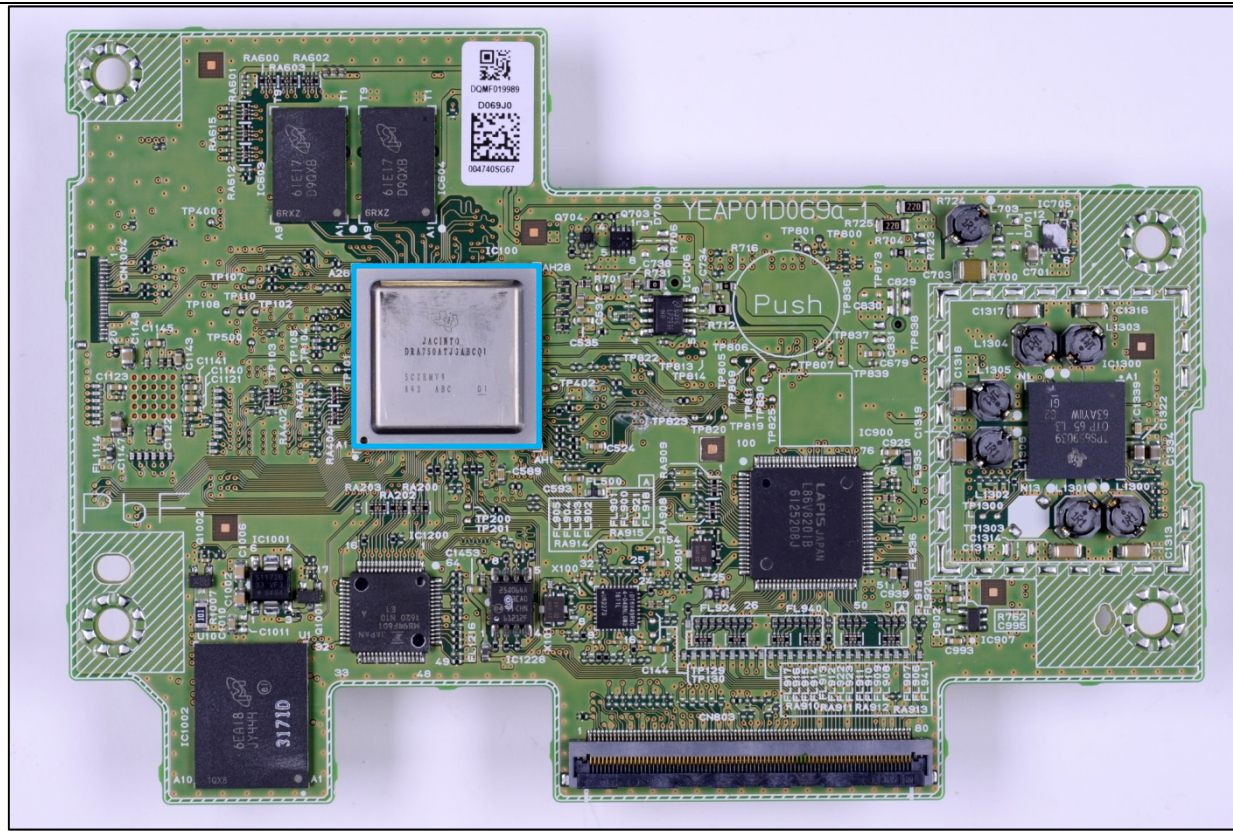
On information and belief, Texas Instruments’ DRA750 SoC is representative of other Texas Instruments infotainment and high-end car information system SoCs having similar functionality (“Accused Texas Instrument Infotainment SoCs”).

The DRA750 SoC is incorporated in downstream products, including without limitation, Panasonic head units, such as Ser. Nos. 130105, 104020, 104069, 500021, which are incorporated in Accused Toyota Navigation units, including Highlander Receiver (86804-0E280), Sienna Navigation Unit (86804-08040), Avalon Navigation Head Unit (86804-07120), and Prius III Navigation System Kit (86804-47330), respectively.

On information and belief the Accused Texas Instrument Infotainment SoCs, and head units and automobiles that incorporate the Accused Texas Instrument Infotainment SoCs infringe directly, indirectly, and or under the doctrine of equivalents, at least claim 1 of the MacInnis ’844 patent.

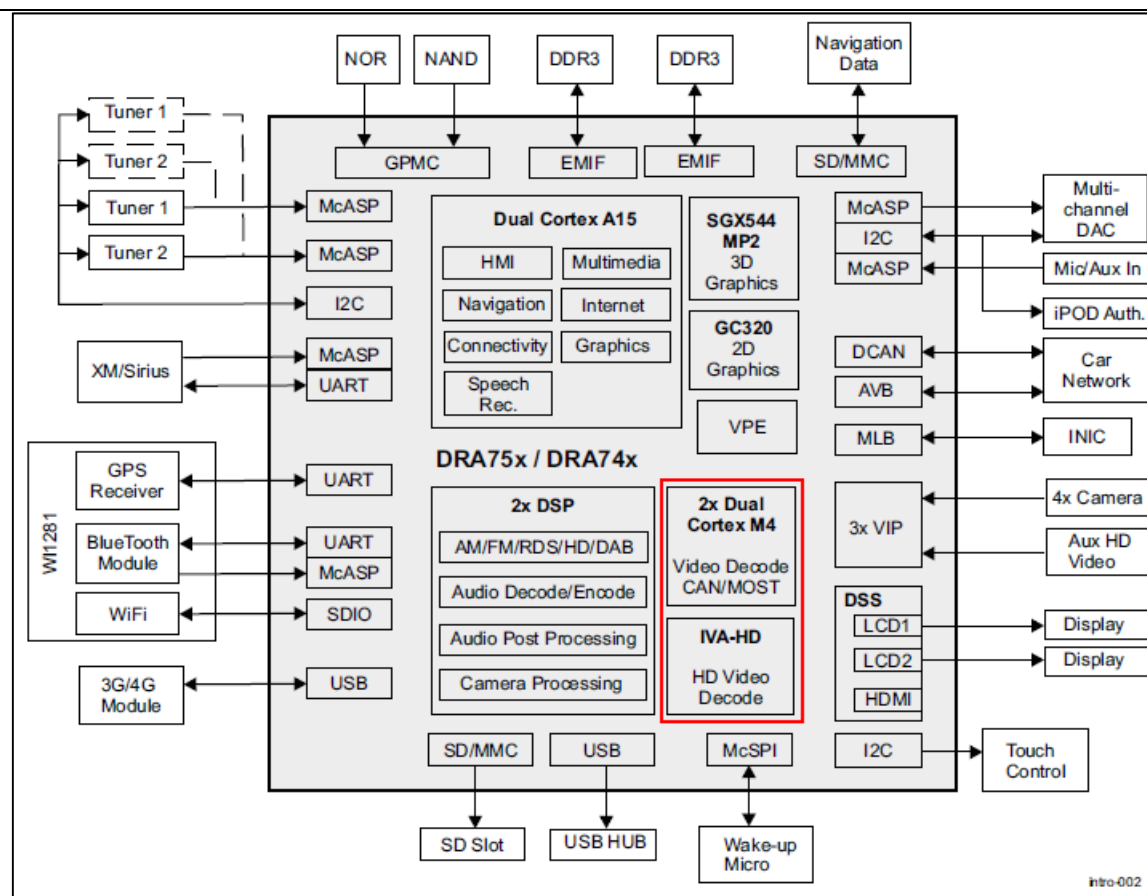
<b>Claim - U.S. Patent No. 8,284,844 (MacInnis)</b>	<b>Application of Claim Language to Accused Product</b>
<b>Claim 1</b>	
A digital media decoding system comprising:	<p>To the extent that the preamble is deemed limiting, the TI DRA750 SoC and downstream products include a digital media decoding system.</p> <p>At least the Panasonic (AT1501) head unit, which is included in at least the Toyota Prius III Navigation System Kit (225202), includes a Texas Instruments DRA750 SoC (highlighted in blue).</p>





The TI DRA750 SoC includes a digital media decoding system.

	<div data-bbox="562 199 1803 573"> <p><b>1.1 DRA75x, DRA74x Overview</b></p> <p>The DRA75x, DRA74x is a high-performance, infotainment application device, based on enhanced OMAP™ architecture integrated on a 28-nm technology.</p> <ul style="list-style-type: none"> <li>• The architecture is designed for advanced graphical HMI and Navigation, Digital and Analog Radio, Rear Seat Entertainment and Multimedia playback, providing Advanced Driver Assistance integration capabilities with Video analytics support, and best-in-class CPU performance, video, image, and graphics processing sufficient to support, among others: <ul style="list-style-type: none"> <li>– Streaming video up to full high definition (Full-HD) (1920×1080p, 60 fps)</li> <li>– 2-dimensional (2D) and 3-dimensional (3D) graphics and composition</li> <li>– Decode of digital radio standards (DAB, HD Radio™), and analog AM/FM/RDS radio</li> <li>– Efficient web browsing</li> </ul> </li> </ul> </div> <p>Ex. 65 – DRA75x, DRA74x Technical Reference Manual at 365.</p>
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Ex. 65 – DRA75x, DRA74x Technical Reference Manual at 367 (annotated).

### How to get Toyota Entune to play videos

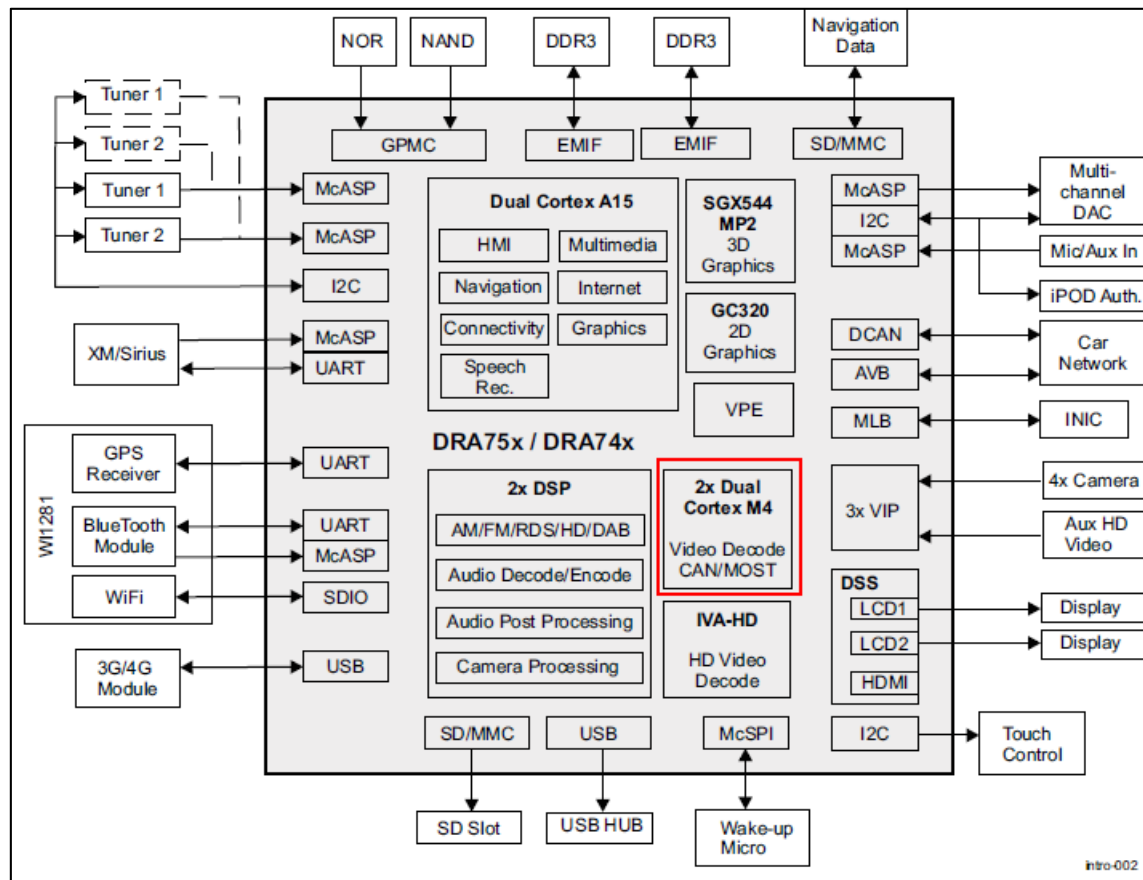
With the **Toyota Entune multimedia system**, drivers are easily able to manage their infotainment apps without taking their eyes from the road or their hands from the wheel. It has made staying connected while driving easier and safer. With the system, drivers are able to access their messages, place phone calls, listen to music and more. While your car may come to a stop, entertainment with **Toyota Entune** doesn't have to. If you're stuck waiting in your Toyota vehicle, you may be interested to learn **how to get Toyota Entune to play videos**.

A lot of Toyota drivers don't even know that their vehicles are able to play videos on their screen. New Toyota vehicles upgraded with the Entune App Suite features a CD player that can also function as an in-dash DVD player.

Ex. 95 – Toyota Website - Entune at 1 (highlighted).

a processor adapted to control a decoding process; and

The TI DRA750 SoC and downstream products include a processor adapted to control a decoding process. For example, the ARM Cortex M4 processors control the “Video Decode” functionality.



Ex. 65 – DRA75x, DRA74x Technical Reference Manual at 367 (annotated).

a hardware accelerator coupled to the processor and adapted to perform a decoding function on

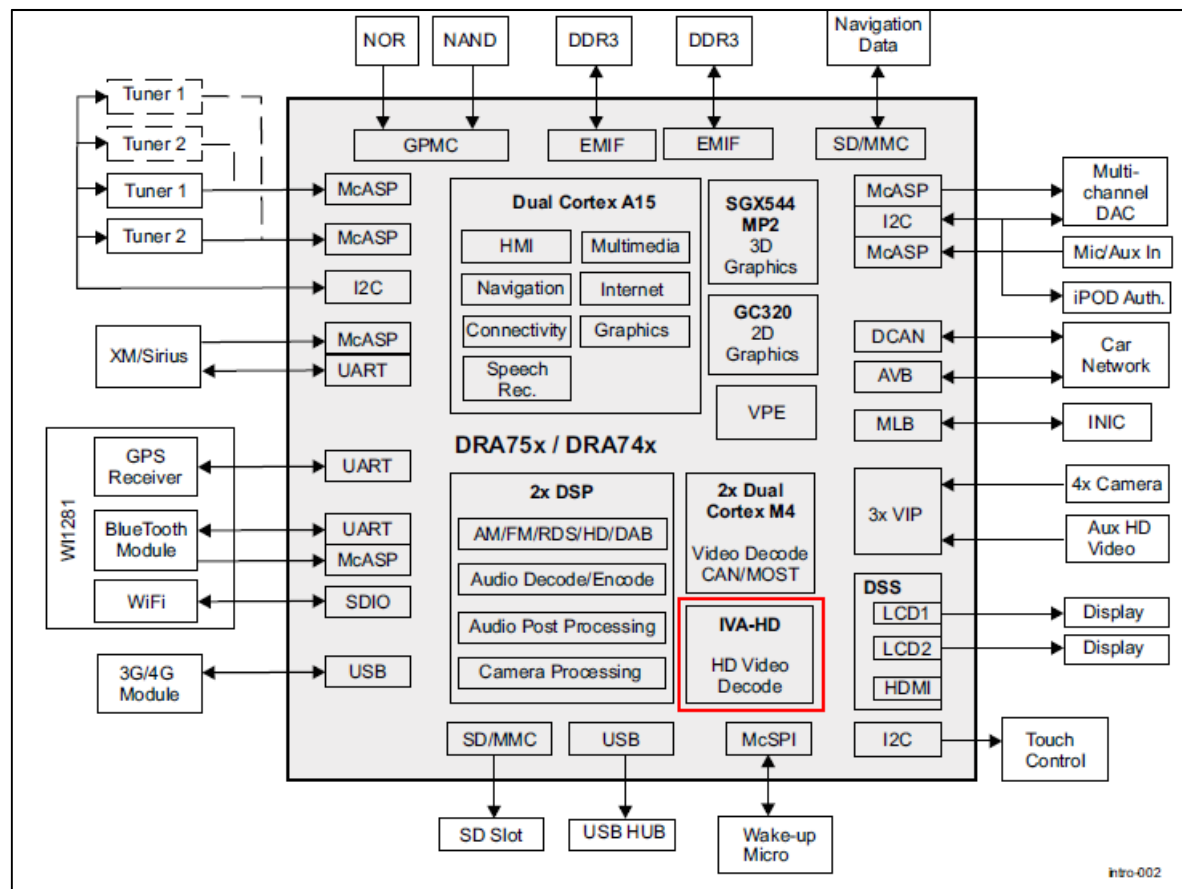
The TI DRA750 SoC and downstream products include a hardware accelerator coupled to the processor and adapted to perform a decoding function on a digital media data stream. For example, the “Image and video accelerator high-definition (IVA-HD) subsystem” includes “a set of video encoder and decoder hardware accelerators.”

a digital media data stream,

### 1.3.5 IVA-HD Subsystem

The IVA-HD subsystem is a set of video encoder and decoder hardware accelerators.

Ex. 65 – DRA75x, DRA74x Technical Reference Manual at 367 (annotated).



Ex. 65 – DRA75x, DRA74x Technical Reference Manual at 367 (annotated).

wherein the accelerator is configurable to

The TI DRA750 SoC and downstream products include a hardware accelerator that is configurable to perform the decoding function according to a plurality of decoding methods.



perform the decoding function according to a plurality of decoding methods.	<p>The TI DRA750 SoC is capable of decoding multiple video compression standards. For example, the TI DRA750 SoC decodes video compressed using the MPEG2, H.264, MPEG4, and VC-1 standards.</p> <div><p><b>Supported Codecs</b></p><p>MJPEG decoder - version 01.00.16.01</p><p>H264 decoder - version 02.00.21.01</p><p>MPEG4 decoder - version 01.00.15.01</p><p>VC1 decoder - version 01.00.02.05</p><p>MPEG2 decoder - version 01.00.17.01</p><p>MPEG4 Encoder - Version 01.00.02.01</p><p>H264 Encoder - Version 02.00.09.01</p><p>MJPEG Encoder - Version 01.00.17.01</p></div> <p>Ex. 71 – Processor SDK Linux Automotive Data Sheet at 29.</p> <p>Decoding MPEG2-compressed video requires performing several of the same decoding functions as MPEG4 requires. Ex. 75, Acton Decl. ¶ 11. Furthermore, decoding MPEG2-compressed video requires performing those functions according to a different method than MPEG4 requires. Ex. 75, Acton Decl. ¶ 11.</p> <p>Therefore, on information and belief, the TI DRA750 SoC comprises a hardware accelerator that “is configurable to perform the decoding function according to a plurality of decoding methods.” Ex. 75, Acton Decl. ¶ 11.</p>
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